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Reddy, E.S.S.; Chandrasekhar, V.; Sashikanth, M.; Kamakoti, V.; Vijaykrishnan, N.;
VLSI Design, 2005. 18th International Conference on
3-7 Jan. 2005 Page(s):736 - 741
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☐ 2. **Multiple errors produced by single upsets in FPGA configuration memory: a possible soluti**
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☐ 3. **Evaluating SEU and crosstalk effects in network-on-chip routers**
Frantz, A.P.; Carro, L.; Cota, E.; Kastensmidt, F.L.;
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10-12 July 2006 Page(s):2 pp.
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☐ 4. **A new reliability-oriented place and route algorithm for SRAM-based FPGAs**
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☐ 5. **On the evaluation of SEU sensitiveness in SRAM-based FPGAs**
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   13-16 March 2001 Page(s):219 - 223
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7. **Using run-time reconfiguration for fault injection in hardware prototypes**
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